CLAIMS.

1.- A pixel module for use in a large-area display, in particular as part of a cluster (118) of a plurality of sequentially interconnected similar pixel modules (120) and driven by a central controller (116), comprising one or more pixel elements (122), characterized in that it further comprises a serial video data bus input (SERIAL IN) and one or more command input lines (CMD's In) electrically connected to inputs of a latch (210) having parallel inputs and outputs and which is clocked with a data clock input (DATA CLK); a current driver device for driving said one or more pixels (122) which is electrically connected to the outputs of latch (210) and to the data clock input (DATA CLK) and which includes a serial output port (SERIAL OUT) for transmitting the serial data to the next pixel module (120) in sequence; a first inverter (214), the output of which (DATA CLK "not") can be used to drive the data clock input (DATA CLK) of the next pixel module (120) in sequence; a grayscale clock (GS CLK) input which is electrically connected to the current driver device (210) and to an output (GS CLK) to drive the gray scale input of the next pixel module (120); an address input (ODD/EVEN) which is electrically connected to a second inverter (216), the output of which (ODD/EVEN "not") can drive the address input (ODD/EVEN) of the next pixel module (120); an EEPROM (218) that is electrically connected to an input port (I^2C BUS) for communication with said central controller (116), which input port is also connected to an output port (I^2C) for connection with the next pixel module (120); and a

power supply (220) input and output.

2.- A pixel module according to claim 1, characterized in that the latch (210) is a multi-bit register.

3.- A pixel module according to claim 1, characterized in that EEPROM (218) stores the color coordinates for each pixel (122) within pixel module (120).

4.- A pixel module according to claim 3, characterized in that the color coordinates are stored in the form of (x,y, Y), where x and y are the coordinates of the primary emitters an Y is the brightness.

5.- A pixel module according to claim 1, characterized in that EEPROM (218) contains production data and factory light output measurement data at the time of manufacture of pixel module (120).

6.- A pixel module according to claim 1, characterized in that EEPROM (218) contains the identification data, the runtime, and the serial number of pixel module (120).

7.- A pixel module according to claim 1, characterized in that communication between EEPROM (218) and the central controller (116) is accomplished using an I^2C bus.

8.- A pixel module according to claim 7, characterized in that said I^2C bus has a standard two wire serial data bus protocol.

9.- A pixel module according to claim 7, characterized in that the I^2C bus has a serial clock line and a serial data line.

10.- A pixel module according to claim 1, characterized in that the power supply comprises a DC/DC converter that provides a DC voltage output for powering latch (210), current driver device (212), first and second inverters (214-216), EEPROM (218), and pixels (122).

11.- A pixel module according to claim 1, characterized in that each pixel (122) includes respectively a red sub-pixel (310), a green sub-pixel (312)and a blue sub-pixel (314), which are separately driven by the current current driver device (212).

12.- A pixel module according to claim 11, characterized in that each sub-pixel (310-312-314) is driven by at least one current source (318) of which the input is connected to an associated shift register (316).

13.- A pixel module according to claim 12, characterized in that each red sub-pixel (310) is driven by at least two current sources (318) which are each connected to an associated shift register (316).

14.- A pixel module according to claim 12 or 13, characterized in that the shift registers (316) of the current driver device are sequentially interconnected, whereby the first shift register (316-01) in the sequence is connected to the latched serial data bus input (SERIAL

IN) and the last shift register (316-16) in the sequence is connected to the serial output port (SERIAL OUT) of the pixel module (120).

15.- A pixel module according to claim 12 or 13, characterized in that the current sources (318) are constant current devices of which the output current can be digitally corrected.

16.- A pixel module according to claim 12 or 13, characterized in that the current sources (318) are formed via a custom ASIC device.

17.- A pixel module according to claim 1, characterized in that the frequency of the data clock input (DATA CLK) is set between 1 to 20 MHz.